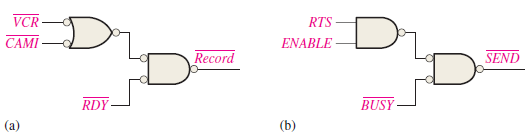
**Assignment- 4**

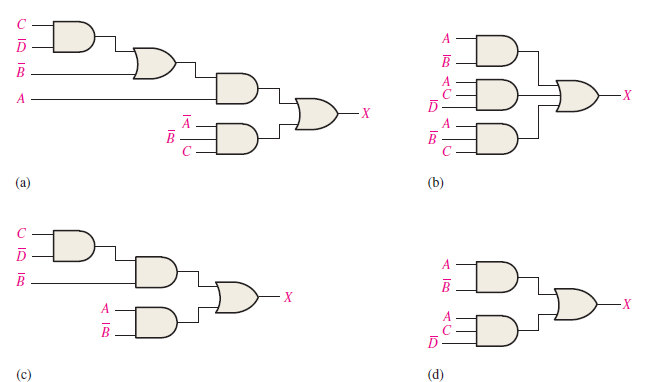
1. Draw the logic circuit represented by each of the following expressions:
2. X= [ AB(C’+D)]’
3. X = (A+B+C’DE’)’+ B’CD’
4. Draw a logic circuit for the case where the output, ENABLE, is HIGH only if the inputs, ASSERT and READY, are both LOW.
5. Draw a logic circuit for the case where the output, HOLD, is HIGH only if the input,

LOAD, is LOW and the input, READY, is HIGH.

1. Develop the truth table for each of the circuits in Figure.



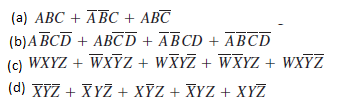
1. Determine which of the logic circuits in Figure are equivalent



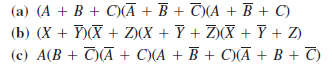
1. Define the domain of each SOP expression in above Problem convert the expression to standard SOP form.

(a) BC’ + DE(B’C + DE) (b) B’C(C D + C) (c) B + C[BD + (C’ + D )E’ ]

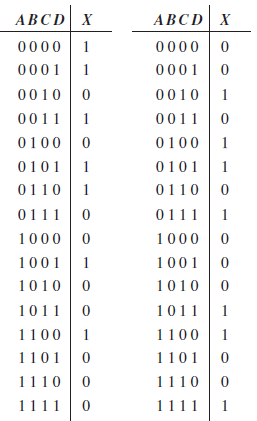
1. Develop a truth table for each of the following standard SOP expressions:



1. Develop a truth table for each of the standard POS expressions:



1. For each truth table in Table, derive a standard SOP and a standard POS expression.



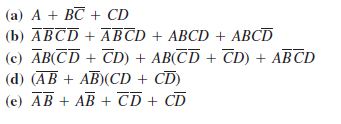
1. Use a Karnaugh map to find the minimum SOP form for each expression:



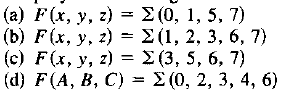
1. Use a Karnaugh map to simplify each expression to a minimum SOP form:



1. Use a Karnaugh map to simplify each expression to a minimum SOP form:



1. Use a Karnaugh map to simplify each Boolean functions.



1. Use a Karnaugh map to simplify each Boolean functions.

